CLAIMS

1. A low voltage differential amplifier architecture with differential input and output signals, comprising,

a first stage comprising a first set of common source connected first identical NMOS transistors and parallel first identical PMOS transistors with their respective gates connected to the differential input signal,

a first current source connected to the sources of the first NMOS transistors and a second current source connected to the sources of the first PMOS transistors,

the drains of the first NMOS transistors are connected to sources of a set of second identical PMOS transistors,

the drains of the first PMOS transistors are connected to sources of a set of second identical NMOS transistors, wherein the second identical PMOS and the second identical NMOS transistors are in a second stage, wherein each of the second identical NMOS transistors and each of the second identical PMOS transistors are symmetrical to each other, and

wherein the drain of one of the second PMOS transistors is connected to the drain of one of the set of second identical NMOS transistors, thereby forming a first current path, and

wherein the drain of the other of the second PMOS transistors is connected to the drain of the other of the set of second identical NMOS transistors, thereby forming a second current path,

wherein the voltage signal between the commonly connected drains defines an intermediate differential output signal,

a first biasing tree including a first tree PMOS transistor and a first tree NMOS transistor, with drains and gates connected to each other, the source of the first tree PMOS connected to the source of the ~~source of the~~ PMOS in the ~~first~~ second current path, wherein the first tree PMOS and the PMOS in the first current path ~~for~~ formed a first current mirror, and the source of the first tree NMOS connected to the source of the NMOS in the

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first current path, wherein the first tree NMOS and the NMOS in the first current path form a second current mirror,

a second biasing tree including a second tree PMOS transistor and a second tree NMOS transistor, with drains and gates connected to each other, the source of the second tree PMOS connected to the source of the ~~source of the~~ PMOS in the ~~second~~ first current path, wherein the second tree PMOS and the PMOS in the second current path form a third current mirror, and the source of the second tree NMOS connected to the source of the NMOS in the ~~second~~ first current path, wherein the second tree NMOS and the NMOS in the second current path form a fourth current mirror,

wherein all the gates of the PMOS and NMOS transistors in the first and the second current paths and in the first and second biasing trees all are connected together,

a third current source connected to the source of the PMOS transistors in the first current path,

a fourth current source connected to the source of the PMOS transistors in the ~~first~~ second current path, wherein the third current source and the fourth current source are equal to each other and each is of a higher value than the second current source,

a fifth current source connected to the sources of the NMOS transistors in the ~~second~~ first current path,

a sixth current source connected to the sources of the NMOS transistors in the second current path, wherein the fifth current source and the sixth current source are equal to each other and each is of a higher value than the first current source,

a third differential stage with a differential input connected to the intermediate differential output, and the third differential stage providing a differential output.

2. The circuit as defined in claim 1 wherein the arrangements of the corresponding sets of transistors and current sources are symmetrical with respect to each other and further comprising the circuit is laid out such that the current paths on either signal path side of the differential topology are identical to each other and further wherein impedances are equal to each other traveling on either signal path side of the differential circuit.

3. The circuit as defined in claim 1 further comprising two buffer inverters each accepting one of the differential output signals and each providing an output suitable for driving a number of loads.

4. A low voltage differential amplifier architecture with differential input and output signals, comprising,

parallel complementary common source first NMOS and first PMOS transistor pairs with their gates accepting the differential input signal,

complementary current sources feeding the source of the first NMOS and first PMOS transistor pairs, the complementary current sources and first NMOS and first PMOS transistor pairs forming a differential input stage, and

a second PMOS pair arranged for accepting the drains of the first NMOS pair,

a second NMOS pair arranged for accepting the drains of the first PMOS pair,

wherein the drains of the second NMOS pair are connected to the corresponding drains of the second PMOS pair forming an intermediate differential output, wherein the second NMOS and PMOS pairs form a folded cascode differential output stage,

a pair of stacked PMOS and NMOS transistor structures with drains connected together, thereby providing complementary biasing current mirroring stacks for the output cascode second NMOS and second PMOS pairs, and further where the all the gates of the second PMOS and second NMOS and stacked PMOS and stacked NMOS transistors are all connect together, and

wherein one of the stacked PMOS sources and the source of one of the second PMOS pair are connected together to a first node, and where the second of the stacked PMOS sources and the source of the other of the second PMOS pair are connected together to a second node, and one of the stacked NMOS sources and the source of one of the second NMOS pair are connected together to a third node, and where the second of the stacked NMOS sources and the source of the other of the second NMOS pair are connected together to a fourth node,

four complementary current sources, one connected to the first node, a second connected to the second node, a third connected to the third node and the fourth connected to the fourth node, and

a third differential stage with a differential input connected to the intermediate differential output, and the third differential stage providing a differential output.

5. The low voltage differential amplifier of claim 4 wherein the first and second current sources are equal to each other and their source complementary current sources are each equal to each other and where each is at least greater than one half the value of the first or second current source.

6. A low voltage differential amplifier of the type having a first stage including a PMOS and NMOS differential transistor pairs and first current sources that are distributed between a low and a high voltage source, the pairs arranged to handle common mode input signals from the low to the high voltage, and wherein the output of the first stage is a differential current that is input to a second stage, wherein the second stage is of the type including parallel paths of first stacked PMOS and NMOS transistors distributed between the low and high voltage sources, and parallel legs of second stacked PMOS and NMOS transistors, each of the second stacked transistors providing a bias for one of the first stacked legs, and wherein the gates of the first and second stacked transistors are connected together, and, furthermore, including four current sources, two between the stacked legs and the high voltage source and two between the low voltage source and the stacked legs, wherein the four current sources are each equal to each other and each is of a value higher ~~that~~ than one half that of each of the first current sources.

7. The differential amplifier of claim 6 further comprising an output differential voltage from the common drains of the first stacked PMOS and NMOS legs, and a third differential amplifier that accepts the differential outputs and provides differential voltage output wherein each of the two differential signals are arranged to traverse from the low to the high voltage sources.